AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 3, line 26, with the following rewritten paragraph:

--The process of Japanese Patent KOKAI No. Hei 11-26394 provides conformal deposit of metal by plating. If there are irregularities on the surface of a seed layer, the deposits on the raised sites may come to contact with adjacent deposits on the sides of the features as the plating proceeds, resulting in formation of voids. Even when the plated film has an appearance of a flat surface due to iodine, seam may be formed in the central portions of the features because the surface is not perfectly ~~plat~~flat.--

Please replace the paragraph beginning at page 14, line 20, with the following rewritten paragraph:

--The organic sulfur compounds are preferably 3-mercapto-1-propanesulfonic acid, 2-mercapto ethane sulfonic acid, bis (~~4-sulfobuthyl~~ 4-sulfobutyl) disulfide, bis (3-sulfopropyl) disulfide, bis (2-sulfoethyl) disulfide, or bis (p-sulfophenyl) disulfide.--

Please replace the table on page 17, with the following rewritten table:

Table 1

Sample No.	Composition of Plating Bath					Plating Condition
	Copper Conc. (mol/L)	Sulfuric Acid Conc. (mol/L)	Hydrochloric Acid Conc. (mol/L)	Type of Additive	Additive Conc. (mol/L) (mg/L)	Current Density (A/dm^2)
1	0.30	1.9	0	A-1	10	1.0
2	0.40	2.0	1.9×10^{-3}	A-3	8	2.5
3	0.80	1.0	0.9×10^{-3}	A-2 B-1 C-1	0.5 100 30	1.0
4	0.30	1.9	1.5×10^{-3}	A-4 B-2 C-4	20 50 30	2.0
5	0.26	1.9	1.9×10^{-3}	A-2 B-2 C-3	1 80 15	0.2
6	0.30	1.9	1.9×10^{-3}	A-2 B-1 C-3	10 40 20	1.5
7	0.80	1.0	1.6×10^{-3}	A-2 B-3 C-3	15 40 10	3.0
8	0.40	1.9	1.9×10^{-3}	A-1 B-4 C-2	8 20 10	1.0
9	0.30	1.9	0	-	-	1.0

Please replace the paragraph beginning at page 19, line 9, with the following rewritten paragraph:

The cross-section of the plated film was observed by a scanning electron microscope (SEM) where the substrate structure after ~~plated~~ plating (Fig. 1C) was processed with FIB (Focused Ion Beam) and the cross-sections of 100 vias were observed. When the process of the growth of copper film to be plated was observed, in the cross-section of the major portion of the interconnection structure as shown in Fig. 3, the thickness of plated film (A) on the surface of the substrate on the way of plating and the thickness of plated film on the bottom of vias (B) were measured and the ratio of B/A was calculated. The uniformity in sheet resistance of plated copper film was evaluated based on measurements at 49 points by a four probe method of the resistivity measurement. Moreover, the test of electromigration resistance (EM resistance) was conducted in the following procedure: a direct current was passed through the interconnections prepared according to the present invention and the resistance was measured with time. Then end of the lifetime was defined at the time when the resistance of the interconnections increased by 30%. Comparisons of the results obtained under various conditions were made. The high EM resistance of the copper interconnections improves the durability of the semiconductor devices themselves. These results are summarized in Table 2 ~~under~~.

Table 2

	Plating Bath Composition		Plating Condition	Evaluation Items			
Sample No.	Type of Dyes	Conc. of Cyanine Dye (mg/L)	Current Density (A/dm^2)	Uniformity in plane of Sheet Resistance (%)	B/A	Presence of ~~boid~~ void	EM Resistance (a.u.)
1	A-1	10	1.0	13	2.1	No	1.4
2	A-3	8	2.5	17	3.0	No	1.5
3	A-2	0.5	1.0	3	2.8	No	4.2
4	A-4	20	2.0	5	3.2	No	5.0
5	A-2	1	0.2	4	5.1	No	5.2
6	A-2	10	1.5	4	4.5	No	6.1
7	A-2	15	3.0	5	5.3	No	4.9
8	A-1	8	1.0	4	6.1	No	5.4
9	-	-	1.0	21	1.0	Yes	1.0

Please replace the table on page 21, with the following rewritten table:

Please replace the paragraph beginning at page 22, line 6, with the following rewritten paragraph:

The plating bath of Sample No. 9 (comparative) produced voids as described later, while those of Sample Nos. 1 to 8 (present invention) did not ~~produced~~ produce observable voids and seams after plating, because of the addition of cyanine dyes to the plating bath allowing the bottoms of the vias to be preferentially plated. Thus, good filling performance could be achieved. Moreover, the EM resistance of the interconnections was also improved. Therefore, it has been found that the semiconductor integrated circuit devices produced according to the present invention have an improved reliability.

Please replace the paragraph beginning at page 23, line 11, with the following rewritten paragraph:

With the copper electroplating bath of Sample No. 9 shown on the bottom in Table 1 as a case of using none of the aforementioned additives which are characteristic of the present invention, copper was plated following to steps shown in Figs. 1A, 1B and 1C ~~shown in the drawings~~.

Please replace the paragraph beginning at page 23, line 17, with the following rewritten paragraph:

The substrate structure after ~~plated~~ plating was processed with FIB in the same manner as above and the cross-sections of 100 vias were observed by SEM. As a result, voids were observed in the copper films in the holes indicating that there

were produced portions not filled with copper in the vias as shown in the cross-sectional view thereof in Fig. 4. Moreover, it was confirmed that some of the voids became smaller into a seam like form.